Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	0	(file adj (upgrade or migration) same (tool or utility)) and ("703"/$.ccls. or "716"/$.ccls.) Rev all	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:12
S62	7	file adj (upgrade or migration) same (tool or utility)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:11
S61	8	map adj file near3 generat$4 same director$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:11
L4	0	(map$4 adj file near3 generat$4 same director$4) and ("703"/$. ccls. or "716"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:11
S59	7	file adj (upgrade or migration) same (tool or utility)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:10
L3	0	file adj (upgrade or migration) same (tool or utility) and ("703"/$. ccls. or "716"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:10
L2	9	(ASIC same directory) and ("703"/$.ccls. or "716"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:09
S58	97	ASIC same directory Scan all	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 17:08
S60	1	compar$6 near2 directories same sort$4 Rev all	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 15:19

S57	3	ASIC same directory same version Rev all	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 14:25
S54	90	ASIC same directory Scan all	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/28 14:25

Google Web Images Groups News Froogle Local[New!] more »
ASIC circuit directory mapping Search Advanced Search Preferences

Web Results **1** - **10** of about **29,400** for **ASIC circuit directory mapping**. (**0.54** seconds)

AnyWho: Internet **Directory** Assistance; Yellow Pages, White Pages ...
... and practical implementation of **circuits**, and the application of **circuit** theoretic
... A commercial EDA portal and **directory** with **ASIC**, FPGA, PCB, ...
www.anywho.com/cgi-bin/webdrill?catkey=gwd/ Top/Computers/CAD_and_CAM/Electronic_Design_Automation - 34k - Cached - Similar pages

AnyWho: Internet **Directory** Assistance; Yellow Pages, White Pages ...
AnyWho is a free **directory** service with residential, business, ... Electronics Design Services firm providing **ASIC**, FPGA, printed **circuit** board (PCB), ...
www.anywho.com/cgi-bin/webdrill?catkey=gwd/ Top/Computers/Consultants/Embedded_Systems - 34k - Cached - Similar pages

Tech **Directory** : **Mapping** Software
... computer technology. Software : Other Appointment Software **ASIC** Catalog Software **Circuit** Board Design ... **Directory** Listing. Title: **Mapping** Software ...
www.tech**directory**.ws/guide/13257.aspx - 10k - Cached - Similar pages

Tech **Directory** : **Mapping** software and services for the creation ...
... **Directory** Listing. Title: **Mapping** software and services for the creation, ... rubbersheeting and maintenance of AutoCAD **maps**; a member of the Autodesk ...
www.tech**directory**.ws/guide/13234.aspx - 10k - Cached - Similar pages
[More results from www.techdirectory.ws]

ED&P Digital System Design Background
... application is known as an application specific integrated **circuit** or **ASIC**.
... The **mapping** from gates to transistors is performed by the CAD tool. ...
www.eng.abdn.ac.uk/~eng186/eg3573/designbackground.htm - 10k - Cached - Similar pages

Description of the SNAP Configuration Control System 1.0 ...
... or an Application Specific Integrated **Circuit** (**ASIC**) is generated. ...
MAP Actel_Name.SEG The top level **directory** also contains the Viewlogic files: ...
sprg.ssl.berkeley.edu/sprite/snap_cm/0_Readme.txt - 14k - Cached - Similar pages

San Francisco Bay Area > Semiconductors in the Yahoo! **Directory**
... the Web | the **Directory** | San Francisco Bay Area ... International Microcircuits, Inc. - Milpitas - manufacturer of integrated **circuits** (clock chips). ...
dir.yahoo.com/.../Business_to_Business/ Electronics/Board_Level_Components/Semiconductors/?o=a - 49k - Cached - Similar pages

Synthesis of an **ASIC** for area,power,delay using Synopsys design ...
... the methodology of optimizing an **ASIC** for parameters like Area,Power and Delay.
... In this window choose Verify Design and Medium level of **Map** Effort. ...
www-ece.engr.utk.edu/~sowmyan/synthesis.html - 17k - Cached - Similar pages

Nimbus ASM Models & Synopsys Synthesis
... in logic synthesis and analysis of **circuit** results for **ASIC** applications. ...
maps your design to the selected target **ASIC** or FPGA device technology, ...
www.cse.sc.edu/~jimdavis/ Tools/exsedia/nimbus_asm_models_.htm - 25k - Cached - Similar pages

Using Both VHDL and Verilog for Board-Level Simulation
... Verilog was originally used for **ASIC** design and verification. ... The steps outlined below are those required for **mapping** a verilog model using ModelSim ...
www.eda.org/fmf/wwwpages/biling.html - 32k - Cached - Similar pages

Gooooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 **Next**

Free! Google Desktop Search: Search your own computer. Download now.
Find: emails - files - chats - web history - media - PDF

ASIC circuit directory mapping Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

©2005 Google

PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: ◉ The ACM Digital Library ○ The Guide

ASIC circuit mapping directory

Search

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used **ASIC circuit mapping directory** Found **11,188** of **154,226**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

☐ Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown Relevance scale

1 Session S6.2: compilers and program analysis: PACT HDL: a C compiler targeting ASICs and FPGAs with power and performance optimizations

Alex Jones, Debabrata Bagchi, Satrajit Pal, Xiaoyong Tang, Alok Choudhary, Prith Banerjee

October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available: pdf(340.93 KB) Additional Information: full citation, abstract, references, index terms

Chip fabrication technology continues to plunge deeper into sub-micron levels requiring hardware designers to utilize ever-increasing amounts of logic and shorten design time. Toward that end, high-level languages such as C/C++ are becoming popular for hardware description and synthesis in order to more quickly leverage complex algorithms. Similarly, as logic density increases due to technology, power dissipation becomes a progressively more important metric of hardware design. PACT HDL, a C to ...

Keywords: ASIC, FPGA, FSM, HDL, IP, SoC, VHDL, Verilog, compiler, high-performance, levelization, low-power, pipelining, synthesis

2 Missing the memory wall: the case for processor/memory integration

Ashley Saulsbury, Fong Pong, Andreas Nowatzyk

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2

Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, citings, index terms

Current high performance computer systems use complex, large superscalar CPUs that interface to the main memory through a hierarchy of caches and interconnect systems. These CPU-centric designs invest a lot of power and chip area to bridge the widening gap between CPU and main memory speeds. Yet, many large applications do not operate well on these systems and are limited by the memory subsystem performance.This paper argues for an integrated system approach that uses less-powerful CPUs that are ...

3 Piranha: a scalable architecture based on single-chip multiprocessing

Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzyk, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese

May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(191.10 KB) Additional Information: full citation, abstract, references, citings, index

terms

The microprocessor industry is currently struggling with higher development costs and longer design times that arise from exceedingly complex processors that are pushing the limits of instruction-level parallelism. Meanwhile, such designs are especially ill suited for important commercial applications, such as on-line transaction processing (OLTP), which suffer from large memory stall times and exhibit little instruction-level parallelism. Given that commercial applications constitute by fa ...

4 Multiway FPGA partitioning by fully exploiting design hierarchy

Wen-Jong Fang, Allen C.-H. Wu

January 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 1

Full text available: pdf(130.36 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a new integrated synthesis and partitioning method for multiple-FPGA applications. Our approach bridges the gap between HDL synthesis and physical partitioning by fully exploiting the design hierarchy. We propose a novel multiple-FPGA synthesis and partitioning method which is performed in three phases: (1) fine-grained synthesis, (2) functional-based clustering, and (3) hierarchical set-covering partitioning. This method first synthesizes a design specification in ...

Keywords: fine-grained synthesis, functional clustering, multi-way partitioning, multiple-FPGA synthesis

5 The sun fireplane system interconnect

Alan Charlesworth

November 2001 **Proceedings of the 2001 ACM/IEEE conference on Supercomputing (CDROM)**

Full text available: pdf(224.87 KB) Additional Information: full citation, abstract, references, citings, index terms

System interconnect is a key determiner of the cost, performance, and reliability of large cache-coherent, shared-memory multiprocessors. Interconnect implementations have to accommodate ever greater numbers of ever faster processors. This paper describes the Sun™ Fireplane two-level cache-coherency protocol, and its use in the medium and large-sized UltraSPARC-III-based Sun Fire™ servers.

6 STiNG: a CC-NUMA computer system for the commercial marketplace

Tom Lovett, Russell Clapp

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2

Full text available: pdf(1.30 MB) Additional Information: full citation, abstract, references, citings, index terms

"STiNG" is a Cache Coherent Non-Uniform Memory Access (CC-NUMA) Multiprocessor designed and built by Sequent Computer Systems, Inc. It combines four processor Symmetric Multi-processor (SMP) nodes (called Quads), using a Scalable Coherent Interface (SCI) based coherent interconnect. The Quads are based on the Intel P6 processor and the external bus it defines. In addition to 4 P6 processors, each Quad may contain up to 4 GBytes of system memory, 2 Peripheral Component Interface (PCI) busses for ...

7 Promises and reality: Server I/O networks past, present, and future

Renato John Recio

August 2003 **Proceedings of the ACM SIGCOMM workshop on Network-I/O convergence: experience, lessons, implications**

Full text available: pdf(225.62 KB) Additional Information: full citation, abstract, references, index terms

Enterprise and technical customers place a diverse set of requirements on server I/O networks. In the past, no single network type has been able to satisfy all of these requirements. As a result several fabric types evolved and several interconnects emerged to satisfy a subset of the requirements. Recently several technologies have emerged that enable a single interconnect to be used as more than one fabric type. This paper will describe the requirements customers place on server I/O networks; t ...

Keywords: 10 GigE, Cluster, Cluster Networks, Gigabit Ethernet, I/O Expansion Network, IOEN, InfiniBand, LAN, PCI, PCI Express, RDMA, RNIC, SAN, Socket Extensions, TOE, iONIC, iSCSI, iSER

8 ASIC microprocessors



M. J. Flynn, R. I. Winner

August 1989 **ACM SIGMICRO Newsletter , Proceedings of the 22nd annual workshop on Microprogramming and microarchitecture**, Volume 20 Issue 3

Full text available: pdf(792.04 KB) Additional Information: full citation, abstract, references, citings, index terms

ASIC microprocessors are becoming an important technology for the control of complex ("embedded") systems. The advantage of such microprocessors is that they can be tailored to the application. This tailoring is quite non-intuitive and optimization is a complex process. Tools such as the Architect's Workbench (AWB) have been developed to assist in this optimization. An example study shows a more than two to one advantage of such assisted analysis.

9 The design of RPM: an FPGA-based multiprocessor emulator



Koray Öner, Luiz A. Barroso, Sasan Iman, Jaeheon Jeong, Krishnan Ramamurthy, Michel Dubois

February 1995 **Proceedings of the 1995 ACM third international symposium on Field-programmable gate arrays**

Full text available: pdf(54.01 KB) Additional Information: full citation, abstract, references, citings, index terms

Recent advances in Field-Programmable Gate Arrays (FPGA) and programmable interconnects have made it possible to build efficient hardware emulation engines. In addition, improvements in Computer-Aided Design (CAD) tools, mainly in synthesis tools, greatly simplify the design of large circuits. The RPM (Rapid Prototype Engine for Multiprocessors) Project leverages these two technological advances. Its goal is to develop a common hardware platform for th ...

Keywords: field-programmable gate arrays, logic emulation, message-passing multicomputers, rapid prototyping, shared-memory multiprocessors

10 An overview of the BlueGene/L Supercomputer



NR Adiga, G Almasi, GS Almasi, Y Aridor, R Barik, D Beece, R Bellofatto, G Bhanot, R Bickford, M Blumrich, AA Bright, J Brunheroto, C Caşcaval, J Castaños, W Chan, L Ceze, P Coteus, S Chatterjee, D Chen, G Chiu, TM Cipolla, P Crumley, KM Desai, A Deutsch, T Domany, MB Dombrowa, W Donath, M Eleftheriou, C Erway, J Esch, B Fitch, J Gagliano, A Gara, R Garg, R Germain, ME Giampapa, B Gopalsamy, J Gunnels, M Gupta, F Gustavson, S Hall, RA Haring, D Heidel, P Heidelberger, LM Herger, D Hoenicke, RD Jackson, T Jamal-Eddine, GV Kopcsay, E Krevat, MP Kurhekar, AP Lanzetta, D Lieber, LK Liu, M Lu, M Mendell, A Misra, Y Moatti, L Mok, JE Moreira, BJ Nathanson, M Newton, M Ohmacht, A Oliner, V Pandit, RB Pudota, R Rand, R Regan, B Rubin, A Ruehli, S Rus, RK Sahoo, A Sanomiya, E Schenfeld, M Sharma, E Shmueli, S Singh, P Song, V Srinivasan, BD Steinmacher-Burow, K Strauss, C Surovic, R Swetz, T Takken,

RB Tremaine, M Tsao, AR Umamaheshwaran, P Verma, P Vranas, TJC Ward, M Wazlowski, W Barrett, C Engel, B Drehmel, B Hilgart, D Hill, F Kasemkhani, D Krolak, CT Li, T Liebsch, J Marcella, A Muff, A Okomo, M Rouse, A Schram, M Tubbs, G Ulsh, C Wait, J Wittrup, M Bae, K Dockser, L Kissel, MK Seager, JS Vetter, K Yates
November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Full text available: pdf(357.61 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper gives an overview of the BlueGene/L Supercomputer. This is a jointly funded research partnership between IBM and the Lawrence Livermore National Laboratory as part of the United States Department of Energy ASCI Advanced Architecture Research Program. Application performance and scaling studies have recently been initiated with partners at a number of academic and government institutions, including the San Diego Supercomputer Center and the California Institute of Technology. This mass ...

11 Benchmarks for layout synthesis—evolution and current status
Krzysztof Koźmiński
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(679.23 KB) Additional Information: full citation, references, citings, index terms

12 Efficient management of memory hierarchies in embedded DRAM systems
Ashley Saulsbury, Su-Jaen Huang, Fredrik Dahlgren
May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.57 MB) Additional Information: full citation, references, index terms

Keywords: COMA, DRAM, cache, latency, memory hierarchy, processor

13 Performance analysis of embedded software using implicit path enumeration
Yau-Tsun Steven Li, Sharad Malik
November 1995 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1995 workshop on Languages, compilers, & tools for real-time systems**, Volume 30 Issue 11

Full text available: pdf(987.85 KB) Additional Information: full citation, abstract, references, citings, index terms

Embedded computer systems are characterized by the presence of a processor running application specific dedicated software. A large number of these systems must satisfy real-time constraints. This paper examines the problem of determining the extreme (best and worst) case bounds on the running time of a given program on a given processor. This has several applications in the design of embedded systems with real-time constraints. An important aspect of this problem is determining which paths in t ...

14 Technology mapping and retargeting for field-programmable analog arrays
Sree Ganesan, Ranga Vemuri
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(137.04 KB) Publisher Site Additional Information: full citation, references, citings, index terms

15 Synthesis and simulation of digital systems containing interacting hardware and

software components
R. K. Gupta, C. N. Coelho, G. De Micheli
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Full text available: pdf(789.92 KB) Additional Information: full citation, references, citings, index terms

16 Optimal clock period FPGA technology mapping for sequential circuits
Peichen Pan, C. L. Liu
July 1998 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 3 Issue 3
Full text available: pdf(252.82 KB) Additional Information: full citation, abstract, references, citings, index terms

We study the technology mapping problem for sequential circuits for look-up table (LUT) based field programmable gate arrays (FPGAs). Existing approaches to the problem simply remove the flip-flops (FFs), then map the remaining combinational logic, and finally put the FFs back. These approaches ignore the sequential nature of a circuit and assume the positions of the FFs are fixed. However, FFs in a sequential circuit can be reposistioned by a functionality-preserving transformation called ...

Keywords: FPGAs, clock period, field-programmable gate arrays, logic replication, look-up tables, retiming, sequential synthesis, technology mapping

17 Technology mapping of sequential circuits for LUT-based FPGAs for performance
Peichen Pan, C. L. Liu
February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**
Full text available: pdf(232.75 KB) Additional Information: full citation, references, citings, index terms

Keywords: FPGAs, clock period, logic replication, look-up table, retiming, sequential circuits, technology mapping

18 High-confidence design for security: don't trust—verify
Shiu-Kai Chin
July 1999 **Communications of the ACM**, Volume 42 Issue 7
Full text available: pdf(180.62 KB) html(27.73 KB) Additional Information: full citation, references, citings, index terms, review

19 S-connect: from networks of workstations to supercomputer performance
Andreas G. Nowatzyk, Michael C. Browne, Edmund J. Kelly, Michael Parkin
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2
Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings, index terms

S-Connect is a new high speed, scalable interconnect system that has been developed to support networks of workstations to efficiently share computing resources. It uses off-the-shelf CMOS technology to directly drive fiber-optic systems at speeds greater than 1 Gbit/sec and can realize bisection bandwidths comparable to high-end MPP systems while being >10x more cost-effective. S-Connect systems do not rely on centralized switches,

but rather are composed of adaptive, topology independen ...

20 Design strategies for controlling standby leakage: An ASIC design methodology with predictably low leakage, using leakage-immune standard cells



Nikhil Jayakumar, Sunil P. Khatri

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(158.00 KB) Additional Information: full citation, abstract, references, index terms

In this paper we introduce a low-leakage standard cell based ASIC design methodology which is based on the use of modified standard cells. These cells are designed to consume *extremely low and predictable* leakage currents in standby mode. For each cell in a standard cell library, we design two low-leakage variants of the cell. If the inputs of a cell during the standby mode of operation are such that the output has a high value, we minimize the leakage in the pull-down network, and vice v ...

Keywords: MTCMOS, leakage current, standard cells, standby current

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2005 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

Results for "((asic)<in>metadata)"
Your search matched **6094** of **1152881** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History
» New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

((asic)<in>metadata)

☐ Check to search only within this results set

Display Format: ◉ Citation ○ Citation & Abstract

Select **Article Information** **View: 1-25** | 26-5

☑ **1. Proceedings. Fourth Annual IEEE International ASIC Conference and Exhibit (Ca 8)**
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International
23-27 Sept. 1991
AbstractPlus | Full Text: PDF(12 KB) **IEEE CNF**

☑ **2. A DSP ASIC design flow based on VHDL and ASIC-emulation**
Andersson, J.;
Design Automation Conference, 1995, with EURO-VHDL, Proceedings EURO-DAC '9
18-22 Sept. 1995 Page(s):562 - 567
AbstractPlus | Full Text: PDF(372 KB) **IEEE CNF**

☐ **3. A high-speed and high-precision Winner-Select-Output (WSO) ASIC**
Haiming Yu; Miyaoka, R.S.; Lewellen, T.K.;
Nuclear Science, IEEE Transactions on
Volume 45, Issue 3, June 1998 Page(s):772 - 776
AbstractPlus | Full Text: PDF(540 KB) **IEEE JNL**

☐ **4. Managing risk in ASIC design cycle**
Zafar, N.;
ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE
17-21 Sept. 1990 Page(s):P1/7.1 - P1/7.3
AbstractPlus | Full Text: PDF(256 KB) **IEEE CNF**

☐ **5. System designer's realization of a core-based ASIC in a comfortable environmen [microcontrollers]**
Conrath, M.C.; Andrietti, B.; Couleur, J.;
ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE
17-21 Sept. 1990 Page(s):P14/3.1 - P14/3.2
AbstractPlus | Full Text: PDF(180 KB) **IEEE CNF**

☐ **6. New delay model for 0.5µ CMOS ASIC**
Gerousis, V.; Nghiem Pan; Weaver, D.;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International
27 Sept.-1 Oct. 1993 Page(s):511 - 514
AbstractPlus | Full Text: PDF(272 KB) **IEEE CNF**

☑ **7. Independence in ASIC design**
Tutcher, J.P.;
Custom VLSI Design and Test, IEE Colloquium on
31 Oct 1988 Page(s):1/1 - 1/4
AbstractPlus | Full Text: PDF(128 KB) **IEE CNF**

☐ **8. Proceedings: The Second Annual IEEE ASIC Seminar and Exhibit (Cat. No.89TH0**
ASIC Seminar and Exhibit, 1989. Proceedings., Second Annual IEEE
25-28 Sept. 1989
AbstractPlus | Full Text: PDF(32 KB) **IEEE CNF**

☐ **9. ASIC technical training-the challenges and opportunities**
Ballinger, N.;
ASIC Seminar and Exhibit, 1989. Proceedings., Second Annual IEEE
25-28 Sept. 1989 Page(s):P14 - 4/1-4
AbstractPlus | Full Text: PDF(252 KB) **IEEE CNF**

☐ **10. A validation strategy for embedded core ASICs**
Hasslen, R.J.; Zafar, N.;
ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE
17-21 Sept. 1990 Page(s):P5/3.1 - P5/3.2
AbstractPlus | Full Text: PDF(176 KB) **IEEE CNF**

☐ **11. Proceedings. Third Annual IEEE ASIC Seminar and Exhibit (Cat. No.90TH0303-8)**
ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE
17-21 Sept. 1990
AbstractPlus | Full Text: PDF(8 KB) **IEEE CNF**

☑ **12. Technology and interconnect simulation for high-speed multi-chip modules**
Gilbert, J.R.;
ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annual IEEE International
21-25 Sept. 1992 Page(s):221
AbstractPlus | Full Text: PDF(60 KB) **IEEE CNF**

☐ **13. Physical design tradeoffs for ASIC technologies**
Banker, J.; Shanbhag, A.; Sherwani, N.;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International
27 Sept.-1 Oct. 1993 Page(s):70 - 78
AbstractPlus | Full Text: PDF(968 KB) **IEEE CNF**

☐ **14. A first pass ASIC development methodology using logic emulation**
Chan, T.; Yeh, B.; Hu, E.;
ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International
19-23 Sept. 1994 Page(s):214 - 218
AbstractPlus | Full Text: PDF(396 KB) **IEEE CNF**

☐ **15. ASIC BIST synthesis: a VHDL approach**
Eberle, T.; McVay, B.; Meyers, C.; Moore, J.;
Test Conference, 1996. Proceedings., International
20-25 Oct. 1996 Page(s):741 - 750
AbstractPlus | Full Text: PDF(856 KB) **IEEE CNF**

☐ **16. A 660 MB/s interface megacell portable circuit in 0.3 µm-0.7 µm CMOS ASIC**
Donnelly, K.; Yiu-Fai Chan; Ho, J.; Chanh Tran; Samir Patel; Lau, B.; Jun Kim; Pak Ch
Wei, J.; Leung Yu; Tarver, R.; Johnson, M.;
Solid-State Circuits Conference, 1996. Digest of Technical Papers. 43rd ISSCC., 1996

International
8-10 Feb. 1996 Page(s):290 - 291, 460
AbstractPlus | Full Text: PDF(1012 KB) **IEEE CNF**

☐ **17. Low power ASIC for high temperature applications**
Vermesan, O.; Rispal, T.; Soulier, L.;
High-Temperature Electronic Materials, Devices and Sensors Conference, 1998
22-27 Feb. 1998 Page(s):81 - 85
AbstractPlus | Full Text: PDF(416 KB) **IEEE CNF**

☐ **18. COST: Circuit Optimization SysTem in ASIC library development environment**
Raghu, C.S.; Bhowmik, S.; Ramani, P.; Sundaram, S.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):460 - 463
AbstractPlus | Full Text: PDF(212 KB) **IEEE CNF**

☐ **19. Partitioning of large HDL ASIC designs into multiple FPGA devices for prototypir verification**
Selvaraj, H.; Sapiecha, P.; Dhavlikar, N.;
Computational Intelligence and Multimedia Applications, 2001. ICCIMA 2001. Proceedi
International Conference on
30 Oct.-1 Nov. 2001 Page(s):411 - 415
AbstractPlus | Full Text: PDF(38 KB) **IEEE CNF**

☐ **20. Low power ASIC design for wireless communications**
McGrath, S.; Scully, E.;
Low Power Analogue and Digital VLSI: ASICS, Techniques and Applications, IEE Colle
2 Jun 1995 Page(s):3/1 - 3/6
AbstractPlus | Full Text: PDF(336 KB) **IEE CNF**

☐ **21. Low-cost simulation of mixed-signal ASIC functionality**
Godfrey, D.M.;
Application Specific Integrated Circuits for Measurement Systems, IEE Colloquium on
24 Feb 1994 Page(s):2/1 - 2/4
AbstractPlus | Full Text: PDF(260 KB) **IEE CNF**

☐ **22. IEE Colloquium on `Processing Issues for VLSI/ASIC Designers' (Digest No.152)**
Processing Issues for VLSI/ASIC Designers, IEE Colloquium on
22 Jun 1992
AbstractPlus | Full Text: PDF(104 KB) **IEE CNF**

☐ **23. Single event upset test structures for digital CMOS application specific integrate**
Baze, M.P.; Bartholet, W.G.; Braatz, J.C.; Dao, T.A.;
Nuclear Science, IEEE Transactions on
Volume 40, Issue 6, Dec 1993 Page(s):1703 - 1708
AbstractPlus | Full Text: PDF(516 KB) **IEEE JNL**

☐ **24. Introduction to CMOS analog standard cell ASIC design**
Bowman, R.J.;
ASIC Seminar and Exhibit, 1989. Proceedings., Second Annual IEEE
25-28 Sept. 1989 Page(s):T2 - 1/1-4
AbstractPlus | Full Text: PDF(224 KB) **IEEE CNF**

☐ **25. Development of an ASIC macrocell design CAD system**
Dahl, L.-M.; Djaja, G.; Mah, L.; Schucker, D.;
ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE
17-21 Sept. 1990 Page(s):P11/1.1 - P11/1.4

AbstractPlus | Full Text: PDF(212 KB) IEEE CNF

View Selected Items

View: 1-25 | 26-5

Help Contact Us Privacy &

Indexed by Inspec

© Copyright 2005 IEEE –

Results for "((asic)<in>metadata)"
Your search matched **6094** of **1152881** documents. You selected **5** items.

e-mail

Download Citations

Choose
Citation

Download
EndNote,ProCite,RefMan

Download

» Learn more

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Display Format: ○ Citation ◉ Citation & Abstract

Article Information View: 1-5 | Vie

1. **Independence in ASIC design**
Tutcher, J.P.
Custom VLSI Design and Test, IEE Colloquium on
31 Oct 1988
Page(s): 1/1-1/4
Summary: Historically OEMs have generally been reluctant to consider the advantages of incc devices into their products because of their perception that ASIC technology is risky, expensive special skills and high volumes. Over th.....
AbstractPlus | Full Text: PDF **IEE CNF**

2. **Proceedings. Fourth Annual IEEE International ASIC Conference and Exhibit (Cat. No.91**
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International
23-27 Sep 1991
Page(s): -
Summary: The following topics are dealt with: ASIC design applications; programmable logic c signal processing ASICs; government and aerospace ASICs; mixed-signal ASIC design; ASIC ASIC technology; very-high-speed integrated
AbstractPlus | Full Text: PDF **IEEE CNF**

3. **Technology and interconnect simulation for high-speed multi-chip modules**
Gilbert, J.R.
ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annual IEEE International
21-25 Sep 1992
Page(s): 221-
Summary: High-performance systems utilizing ASICs must consider the ASIC interconnection and signal quality. ASIC-to-ASIC interconnection is often the limiting factor. A systematic, modu SPICE modeling and simulation is describe.....
AbstractPlus | Full Text: PDF **IEEE CNF**

4. **Single event upset test structures for digital CMOS application specific integrated circui**
Baze, M.P.; Bartholet, W.G.; Braatz, J.C.; Dao, T.A.
Nuclear Science, IEEE Transactions on
Volume: 40 Issue: 6 Dec 1993
Page(s): 1703-1708
Summary: A test structure methodology for digital CMOS ASICs (application-specific integrate can be used to evaluate the hardness of various ASIC libraries and processes is described. Th identifies categories of ASIC cells and uses a s.....
AbstractPlus | Full Text: PDF **IEEE JNL**

5. **A DSP ASIC design flow based on VHDL and ASIC-emulation**
Andersson, J.
Design Automation Conference, 1995, with EURO-VHDL, Proceedings EURO-DAC '95., Europ
18-22 Sep 1995
Page(s): 562-567
Summary: In an ASIC project VHDL-simulation, VHDL-synthesis and ASIC-emulation has bee

project is completed and described in this paper. As an introduction a short presentation of the MINI-LINK, is given. The project started with a rou.....

AbstractPlus | Full Text: PDF **IEEE CNF**

View: 1-5 | View Search Res

Help Contact Us Privacy &

Indexed by Inspec®

© Copyright 2005 IEEE –